The

Patent IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

pplicant(s): André DeHon, et al.) Re: Information Disclosure Statement

Serial No.: 10/643,772) Group: 2825

Filed: August 18, 2003) Examiner: not yet assigned

Our Ref: B-5138NP 621046-7

For: "ELEMENT PLACEMENT METHOD AND

APPARATUS"

) Date: April 7, 2005

Commissioner for Patents P.O. Box 1450 Alexandria VA, 22313-1450

Sir:

In accordance with the Applicants' duty to disclose information which may be material to the examination of this application, the undersigned respectfully requests that the Examiner consider on the merits the documents listed on the enclosed Form PTO-1449 (modified) before issuing the first Office Action on the merits. Copies of the foreign patent documents and the non-patent publications listed on the enclosed Form PTO-1449 (modified) are enclosed herewith for the Examiner's convenience. Copies of the U.S. patent documents listed on the enclosed Form PTO-1449 (modified) are not enclosed, pursuant to Deputy Commissioner Stephen G. Kunin's Pre OG Notice dated July 11, 2003.

The documents listed on the enclosed Form PTO-1449 (modified) include those cited in the International Search Report for the corresponding PCT Application No. PCT/US03/25941. A copy of the Search Report (4 pages) is enclosed herewith.

The documents listed on the enclosed Form PTO-1449 (modified) include those cited in the International Search Report for a related PCT Application No. PCT/US03/02864. A copy of the Search Report (4 pages) is enclosed herewith.

WIPO International Publication Document No. WO 98/35294 is not in English. A concise English-language explanation of the relevance of WIPO International Publication Document No. WO 98/35294 can be found in the enclosed English-language abstract.

It should be noted that the above-identified application may be related by subject matter to the following U.S. Application(s): 10/356,710, filed January 31, 2003 (published as U.S. Patent Application Publication No. 2003/0174723 A1); and 10/897,582, filed July 23, 2004 (published as U.S. Patent Application Publication No. 2005/0063373 A1). Pursuant to 37 C.F.R. 1.56(a) and M.P.E.P. 2004, paragraph 9, the applicant brings these copending applications to the attention of the Examiner. The Examiner should consider this information during the prosecution of the above-identified application. However, citation of these applications does not constitute an admission that the claims of the present application are substantially similar or similar to those of the applications listed above.

The filing of this Information Disclosure Statement (IDS) shall not be construed as a representation that a search has been made (37 C.F.R. 1.97(g)), an admission that the information cited is, or is considered to be, material to patentability, or that no other material information exists.

The Applicants believe that this IDS is being submitted before the issuance of a first Office Action on the merits and before the issuance of a Final Rejection or Notice of Allowance. Therefore, no official fees should be due; and this IDS should be considered on the merits. If this IDS is being submitted after the issuance of the first Office Action on the merits and before the issuance of a Final Rejection or Notice of Allowance, please contact the

undersigned to authorize a payment of \$180.00 (or any other required amount), which is the fee set forth in 37 C.F.R. § 1.97(c), if the Examiner believes that such a fee is due in order for this IDS to be considered on the merits.

The filing of this Information Disclosure Statement shall not be construed as an admission against interest in any manner. (Notice of January 9, 1992, 1135 O.G. 13-25, at 25.)

The person making this statement is the practitioner who signs below on the basis of information supplied by an individual associated with the filing and prosecution of this application (37 C.F.R. § 1.56(c)) and on the basis of information in the practitioner's file.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first-class mail in an envelope addressed to the "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450", on April 7, 2005 by Shana Morda.

Robert Popa Attorney for Applicant

Respectfully submitted,

Reg. No. 43,010

5670 Wilshire Boulevard Suite 2100 Los Angeles, CA 90036 (323) 934-2300

LADAS & PARRY

Enclosures: Form PTO-1449 (modified) (3 pages)

Copy of Search Report for PCT/US03/25941 (4 pages) Copy of Search Report for PCT/US03/02864 (4 pages) Copy of Non-U.S. Patent documents listed on Form PTO-

1449 (modified)

Form PTO-1449 (Modified) Page 1 of 3	ATTY DOCKET NO. B-5138NP 621881-3	U.S. SERIAL NO. 10/643,772	
LIST OF PATENTS AND PUBLICATIONS STATEMENT	APPLICANTS André DeHon, et al.		
STATEMENT	FILING DATE August 18, 2003	GROUP 2825	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	ISSUE DATE	NAME	CLASS	SUB- CLASS	FILING DATE or 102(e) DATE IF APPROPRIATE
	3,654,615	4/1972	Freitag	340	172.5	
	5,495,419	2/1996	Rostoker et al.	364	468	
	6,243,851 B1	6/2001	Hwang et al.	716	10	<u> </u>
	2003/0174723 A1	9/2003	DeHon et al.	370	404	
	2005/0063373 A1	3/2005	DeHon et al.	370	380	

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES/NO
	98/35294	8/1998	WO			abstract

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Arora, S., et al., "On-Line Algorithms For Path Selection In A Nonblocking Network," SIAM Journal on Computing, Vol. 25, No. 3, pp. 1-25 (June 1996).	
Banerjee, P., et al., "A Parallel Simulated Annealing Algorithm for Standard Cell Placement on a Hypercube Computer," IEEE International Conference on Computer-Aided Design, pp. 34-37 (1986).	
Banerjee, P., et al., "Parallel Simulated Annealing Algorithms for Cell Placement on Hypercube Multiprocessors," IEEE Transactions on Parallel and Distributed Systems, Vol. 1, No. 1, pp. 91-106 (1990).	
Bhatt, S.N., et al., "A Framework for Solving VLSI Graph Layout Problems," Journal of Computer and System Sciences, Vol. 28, pp. 300-345 (1984).	
Chan, P.K., et al., "Acceleration of an FPGA Router," Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines, IEEE, pp. 175-181 (April 1997).	
Chan, P.K., et al., "New Parallelization and Convergence Results for NC: A Negotiation-Based FPGA Router," Proceedings of the 2000 International Symposium on Field-Programmable Gate Arrays (FPGA '00), ACM/SIGDA, pp 165-174 (February 2000).	
Chong, F., et al., "METRO: A Router Architecture for High-Performance, Short-Haul Routing Networks," Proceedings of the Annual International Symposium on Computer Architecture, Chicago, IEEE, Vol. SYMP. 21, pp 266-277 (April 18-21, 1994).	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449 (Modified) Page 2 of 3	ATTY DOCKET NO. B-5138NP 621881-3	U.S. SERIAL NO. 10/643,772		
LIST OF PATENTS AND PUBLICATIONS	APPLICANTS André DeHon, et al.			
STATEMENT	FILING DATE August 18, 2003	GROUP 2825		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)
	Dally, W.J., "Express Cubes: Improving the Performance of k -ary n -cube Interconnection Networks," IEEE Transactions on Computers, Vol. 40, No. 9, pp. 1016-1023 (September 1991).
	DeHon, A., "Balancing Interconnect and Computation in a Reconfigurable Computing Array (or why you don't really want 100% LUT utilization)," Proceedings of the 1999 ACM/SGDA Seventh International Symposium on Field Programmable Gate Arrays, pp. 1-10 (February 21-23, 1999).
	DeHon, A., "Compact, Multilayer Layout for Butterfly Fat-Tree," Proceedings of the Twelfth ACM Symposium on Parallel Algorithms and Architectures, 10 pages total (July 2000).
	DeHon, A., "Entropy, Counting and Programmable Interconnect," FPGA'96, ACM-SIGDA Fourth International Symposium on FPGAs, Monterey CA, Fig. 2, 7 pages total (February 11-13 1996).
	DeHon, A., "Rent's Rule Based Switching Requirements, System Level Interconnect Prediction," SLIP 2001, pp. 197-204 (March 31-April 1, 2001).
	Erényi, I., et al., "FPGA-based Fine Grain Processor Array Design Considerations," Proceedings of the Third IEEE International Conference, pp. 659-662 (1996).
	Fiduccia, C.M., et al., "A Linear-Time Heuristic for Improving Network Partitions," 19th Design Automation Conference, Paper 13.1, pp. 175-181 (1982).
	Greenberg, R.I., et al., "A Compact Layout for the Three-Dimensional Tree of Meshes," Appl. Math. Lett., Vol. 1, No. 2, pp. 171-176 (1988).
	Greenberg, R.I., et al., "Randomized Routing on Fat-Trees," Laboratory for Computer Science, Massachusetts Institute of Technology, Cambridge, Massachusetts, pp. 1-23 (June 13, 1996).
	Henry, D.S., et al., "Cyclic Segmented Parallel Prefix," <i>Ultrascalar Memo 1</i> , Yale, pp. 1-14 (November 1998).
	Horvath, E.I, "A Parallel Force Direct Based VLSI Standard Cell Placement Algorithm," Proceedings of the International Symposium on Circuits and Systems, Vol. 2, pp. 2071-2074 (1993).
	Iosupovici, A., "A Class of Array Architectures for Hardware Grid Routers," <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , Vol. CAD-5, No. 2, pp. 245-255 (April 1986).
	Kernighan, B.W., et al., "An Efficient Heuristic Procedure for Partitioning Graphs," Bell Syst. Tech. J., Vol. 49, No. 2, pp. 76-80 (February 1970).
,	Landman, B.S., et al., "On Pin Versus Block Relationship for Partitions of Logic Graphs," IEEE Transactions on Computers, Vol. C-20, No. 12, pp. 1469-1479 (1971).

BXAMINER	DATE CONSIDERED	

Form PTO-1449 (Modified) Page 3 of 3	ATTY DOCKET NO. B-5138NP 621881-3	U.S. SERIAL NO. 10/643,772	
LIST OF PATENTS AND PUBLICATIONS	APPLICANTS André DeHon, et al.		
STATEMENT	FILING DATE August 18, 2003	GROUP 2825	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

∥ s	eiserson, C.E., "Fat Trees: Universal Networks for Hardware-Efficient Supercomputing," <i>IEEE Transactions on Computers</i> , Vol.C-34, No. 10, pp. 892-901 October 1985).
F	CMurchie, L., et al., "PathFinder: A Negotiation-Based Performance-Driven Router for PGAs," Proceedings of the ACM/SIGDA International Symposium on Field-Programmable Sate Arrays, ACM, pp. 111-117 (February 1995).
I <	METIS: Family of Multilevel Partitioning Algorithms," NTERNET: http://www-users.cs.umn.edu/~karypis/metis/index.html> page total (Retrieved on February 4, 2005).
	yan, T., et al., "An ISMA Lee Router Accelerator," <i>IEEE Design and Test of</i> Computers, pp 38-45 (October 1987).
	Gai-Halasz, G.A., "Performance Trends in High-End Processors," Proceedings of the REEE, Vol. 83, No. 1, pp. 20-36 (January 1995).
I <	SS7 Tutorial," Performance Technologies, INTERNET: Inttp://www.pt.com/tutorials/ss7> Op. 1-23 (August 22, 2001).
t	Swartz, J.S., et al., "A Fast Routability-Driven Router for FPGAs," Proceedings of the 1998 International Symposium on Field-Programmable Gate Arrays (FPGA '98), pp. 40-149 (February 1998).
	Pessier, R., "Negotiated A* Routing for FPGAs," Proceedings of the 5th Canadian Workshop on Field Programmable Devices, 6 pages total (June 1998).
	Chompson, C.D., "Area-Time Complexity for VLSI," Eleventh Annual ACM Symposium on Theory of Computing, pp. 81-88 (May 1979).
	Cogawa, N., et al., "An Incremental Placement and Global Routing Algorithm for Field-Programmable Gate Arrays," Design Automation Conference, pp. 519-526 (1998).
R	Cogawa, N., et al., "Maple: A Simultaneous Technology Mapping, Placement, and Global Routing Algorithm for Field-Programmable Gate Arrays," IEEE/ACM International Conference on Computer-Aided Design, pp. 156-163 (1994).
P	Psu, W., et al., "HSRA: High-Speed, Hierarchical Synchronous Reconfigurable Array," Proceedings of the International Symposium on Field Programmable Gate Arrays, pp 1-10 (February 1999).
{	Nu, Yu-Liang, et al., "Graph-Based Analysis of 2-D FPGA Routing," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 15, No. 1, pp. 33-14 (January 1996).

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.